



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/605,092      | 09/08/2003  | Satoshi Kitamura     | SIC-03-035          | 2091             |

29863 7590 07/13/2006

DELAND LAW OFFICE  
P.O. BOX 69  
KLAMATH RIVER, CA 96050-0069

EXAMINER

PARRIES, DRUM

|          |              |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2836

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/605,092

**Applicant(s)**

KITAMURA ET AL.

**Examiner**

Dru M. Parries

**Art Unit**

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 15 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>5-15-06</u> .   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-37 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-7 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366) and Nakabayashi et al. (JP 04-150729 A). Turner teaches a bicycle power supply comprising an AC power supply (172) supplying power to a variety of electrical components (160-168; 174-184) through a plurality of batteries (170). He also teaches a rectifier (154) that converts the AC power to DC current to supply power to the plurality of storage elements. He also teaches some of the electrical components to be a mechanical adjusting mechanism (166, 168) (i.e. transmission or suspension), a microprocessor (150) and a sensor element (184) where the mechanical adjusting mechanism has a higher capacitance than the microprocessor. Turner fails to teach separate storage elements providing power to separate electrical components and a unit that prevents power flow from one storage element to another. Nakabayashi teaches two different storage elements (1st - 7 and 2nd - 12, 13) in parallel each structured to supply power to its own electrical component (10 and 16). He also teaches a

Art Unit: 2836

power-inhibiting unit (11) to prevent power flow from the first storage element to the second component and from the second storage element to the first component. He also teaches reverse current inhibiting unit (15) coupled between the first and second storage elements to inhibit flow from the second storage element to the first. He also teaches that current flows from the first storage element to the second via the reverse current inhibiting unit. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the plurality of batteries to supply power to their own individual loads (i.e. the first storage element supplying power to the mechanical adjusting mechanism and the second storage element supplying power to the microprocessor and/or a sensor element) to be able to supply precise output values to each component in the system thereby creating a more efficient system. It also would have been obvious to one of ordinary skill in the art at the time of the invention to use the power and reverse current inhibiting units to eliminate stray currents that may cause malfunction in the system.

4. Claims 8, 16-19, 22-25, 27-32, and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366) and Nakabayashi et al. (JP 04-150729 A) as applied to claims 1 and 4-7 above, and further in view of Mitchell (6,355,990). Turner and Nakabayashi teach a bicycle power supply system as described above. They fail to teach a power switch unit that selectively switches current to a storage element in response to the voltage at that storage element and a voltage stabilizing circuit. Mitchell teaches a power switch unit (S1, S2, S3....Sn) that selectively switches current to the first split first storage element (C1) via switch (S1) and second split first storage element (C2) via switch (S2) in response to a voltage measured at the

Art Unit: 2836

respective storage element. Mitchell teaches an unlimited amount of switches and storage elements (i.e. a first split second and second split second storage elements) for the plurality of loads that all work the same way as C1, C2, S1, and S2. The power switch unit is used to stabilize the voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the power switches of Mitchell's invention into Turner's system so that each storage element will have the right amount of stored voltage to power each individual load.

5. Claims 14, 15, 20, 21, 26, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366), Nakabayashi et al. (JP 04-150729 A), and Mitchell (6,355,990) as applied to claims 1, 4, 5, 13, 16, 19, 23-25, 31 and 32 above, and further in view of Yoshimi (JP 01-318519 A). Turner, Nakabayashi, and Mitchell teach a bicycle power supply as described above. They all fail to teach diodes between the power switch unit and each storage element. Yoshimi teaches reverse current inhibiting diodes (3-1, 3-2,...3-n) between switches (2-1, 2-2,...2-n), connected to an input, and an output. It would have been obvious to one of ordinary skill in the art at the time of the invention to place reverse current inhibiting diodes between the power switches and the storage elements so that no stray current will flow backward in the system when trying to charge the storage elements and possibly cause malfunction or incorrect voltages in other storage elements or electrical components.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The

Art Unit: 2836


examiner can normally be reached on Monday -Thursday from 8:00am to 5:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached on 571-272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

6-28-2006



BRIAN SIRCUS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2836